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| 09/843,465 | 04/25/2001 | Michael Ginsberg | MS1-720US | 8323 |

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| EXAMINER | |
|---|---|
| ALI, SYED J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2127 | |

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/843,465 | GINSBERG, MICHAEL | |
| | Examiner | Art Unit | |
| | Syed J Ali | 2127 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 25 April 2001.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 April 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-29 are pending in this application.

### *Claim Objections*

2. **Claims 8 and 22 are objected to because of the following informalities:**

   a. In line 11 of claim 8, "the a set of threads" should read "a set of threads".

   b. In line 4 of claim 22, "and," should read "and".

   Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 5, 7, 11, 14, 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

5. The following claim language is indefinite:

   a. As per claims 5 and 11, it is unclear how "wherein the scheduling" is meant to limit the claim.

   b. As per claims 7, 14, and 21, it is unclear if the claims are independent or dependent claims. As is, "computer-readable media" claims cannot depend from

"method" claims, nor can a "computer" claim depend from a "computer-readable media" claim.

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-4, 6-10, 12-23, and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toll et al. (USPN 6,308,279) (hereinafter Toll).**

8. As per claim 1, Toll teaches the invention as claimed, including a method for providing thread scheduling in a device, the device comprising one or more hardware elements operatively coupled to an operating system comprising a plurality of program modules, the method comprising:

scheduling one or more threads according to a predetermined periodic rate (col. 2 lines 22-28; col. 3 lines 38-45);

determining whether or not there are any threads to execute (col. 2 lines 32-34; col. 3 lines 8-12); and

responsive to a determination that there are no threads to execute, deactivating at least one subset of components for a dynamic variable amount of time (col. 2 lines 32-34; col. 3 lines 8-12), the one subset being selected from a group of components comprising

the hardware elements and the program modules (col. 2 lines 32-34), the dynamic variable amount of time being independent of the predetermined periodic rate and being based on a sleep state of a set of threads (col. 3 lines 23-30).

9. Although Toll does not specifically state that the sleeping threads are in a sleep queue, the use of sleep queues for blocked or sleeping threads is well known and expected in the art. In typical applications, a thread may enter a sleep queue if it is waiting on a synchronization construct, or otherwise needs to block awaiting a particular event. The use of a sleep queue is used so that when the shared resource becomes available, the highest priority thread can be dispatched, thus increasing the real-time capabilities of the system. It would have been obvious to one of ordinary skill in the art to include a sleep queue for the blocked threads, such that when the system returns out of the low power mode, the most critical threads may be serviced first.

10. As per claim 2, Toll teaches the invention as claimed, including a method as recited in claim 1, wherein the dynamic variable amount of time is based on a maximum amount of time that a thread can yield before needing to be scheduled for execution (col. 3 lines 15-18; col. 3 lines 30-34).

11. As per claim 3, Toll teaches the invention as claimed, including a method as recited in claim 1, wherein the device is a battery powered device (col. 1 lines 11-24).

12. As per claim 4, "Official Notice" is taken that although Toll does not specifically teach a method as recited in claim 1, wherein the operating system comprises an operating system selected from a group of operating systems comprising Microsoft WINDOWS CE, Linux, WindRiver, QNX, or PALM operating systems, the use of these operating systems is well known and expected in the art. Toll specifically addresses the issue of the need for extending battery life in mobile computing devices (col. 1 lines 11-24). In modern computing, handheld devices have become prevalent, wherein most handheld devices run on one of the claimed operating systems. The operating system specifically mentioned by Toll is taught in a more general sense, as one that supports multi-threading, and uses the scheduling of these threads as the control for preserving battery power. Since all of the claimed operating systems are multithreaded, there is inherent support for the power mode transition method disclosed by Toll.

13. As per claim 6, Toll teaches the invention as claimed, including a method as recited in claim 1:

wherein the providing further comprises setting a system timer to generate a notification at the predetermined periodic rate (col. 3 lines 15-34);

wherein the deactivating further comprises resetting the system timer to generate the notification after the dynamic variable amount of time has elapsed since the deactivating (col. 3 lines 15-34); and

wherein the method further comprises:

receiving the notification after the dynamic variable amount of time has elapsed since the deactivating (col. 3 lines 15-34); and

responsive to the receiving:

resetting the system timer to generate the notification at the predetermined periodic rate (col. 3 lines 15-34); and

activating the at last one subset of components (col. 3 lines 15-34).

14. As per claim 7, Toll teaches the invention as claimed, including one or more computer-readable media containing a computer executable program that performs a method as recited in claim 1 (Claim 21).

15. As per claim 8, Toll teaches the invention as claimed, including a method for providing thread scheduling in a device, the device comprising one or more hardware elements operatively coupled to an operating system comprising a plurality of program modules, the method comprising:

scheduling one or more threads at a predetermined periodic rate (col. 2 lines 22-28; col. 3 lines 38-45);

determining whether or not there are any threads to execute (col. 2 lines 32-34; col. 3 lines 8-12); and

responsive to a determination that there are no threads to execute, deactivating at least one subset of components for a dynamic variable amount of time (col. 2 lines 32-34; col. 3 lines 8-12), the one subset being selected from a group of components comprising the hardware elements and the program modules (col. 2 lines 32-34), the dynamic variable amount of time being based on a sleep state of a set of threads and independent of the predetermined periodic rate (col. 3 lines 23-30); and

activating the one subset of components only when the operating system needs to perform an action selected from a group of actions comprising scheduling a thread for execution upon expiration of the dynamic variable amount of time since the deactivating, or upon receipt of an external event, processing the external event, wherein the external event is not a system timer event (col. 3 lines 15-34).

16. The absence of a teaching of a "sleep queue" within Toll is discussed above in reference to paragraph 9.

17. As per claim 9, Toll teaches the invention as claimed, including a method as recited in claim 8, wherein the device comprises a battery powered device (col. 1 lines 11-24).

18. As per claim 10, "Official Notice" is taken that the use of the Microsoft WINDOWS CE operating system would have been an obvious modification to Toll for reasons discussed above in reference to paragraph 12.

19. As per claim 12, Toll teaches the invention as claimed, including a method as recited in claim 8:

wherein the scheduling further comprises setting a system time to the predetermined periodic rate, the predetermined periodic rate corresponding to a thread scheduling accuracy (col. 3 lines 15-34); and

wherein the deactivating further comprises resetting the system timer to generate a notification after the dynamic variable amount of time has elapsed since the deactivating (col. 3 lines 15-34).

20. As per claim 13, Toll teaches the invention as claimed, including a method as recited in claim 8:

wherein the deactivating further comprises resetting a system timer to generate a notification after the dynamic variable amount of time has elapsed, the dynamic variable amount of time being a maximum amount of time that a thread can yield to other threads before needing to be scheduled for execution (col. 3 lines 15-34); and

wherein the activating further comprises resetting the system timer to the predetermined periodic rate to provide substantial thread scheduling accuracy (col. 3 lines 15-34).

21. As per claim 14, Toll teaches the invention as claimed, including one or more computer-readable media containing a computer executable program that performs a method as recited in claim 8 (Claim 21).

22. As per claim 15, Toll teaches the invention as claimed, including a computer-readable storage medium containing computer-executable instructions for scheduling threads in a device, the device including an operating system comprised of a plurality of program modules that are in turn coupled to one or more hardware elements, the computer-executable instructions comprising instructions for:

determining at a periodic rate whether or not there are any threads to execute (col. 2 lines 22-34; col. 3 lines 8-12; col. 3 lines 38-45); and

responsive to a determination that there are no threads to execute, deactivating at least one subset of components for a dynamic variable amount of time (col. 2 lines 32-34; col. 3 lines 8-12), the at least one subset being selected from a group of components comprising the one or more of the program modules and one or more of the hardware elements (col. 2 lines 32-34), the dynamic variable amount of time being independent of the periodic rate, the dynamic variable amount o time being based on a sleep state of a set of threads (col. 3 lines 23-30).

23. The absence of a teaching of a "sleep queue" within Toll is discussed above in reference to paragraph 9.

24. As per claim 16, Toll teaches the invention as claimed, including a computer-readable storage medium, as recite in claim 15, wherein the dynamic variable amount of time comprises a maximum amount of time that a thread has specified that it will yield to other threads before it needs to be scheduled for execution (col. 3 lines 15-18; col. 3 lines 30-34).

25. As per claim 17, Toll teaches the invention as claimed, including a computer-readable storage medium as recited in claim 15, wherein the device comprises a battery powered device (col. 1 lines 11-24).

26. As per claim 18, "Official Notice" is taken that the use of the Microsoft WINDOWS CE operating system would have been an obvious modification to Toll for reasons discussed above in reference to paragraph 12.

27. As per claim 19, Toll teaches the invention as claimed, including a computer-readable storage medium as recited in claim 15, wherein the computer-executable instructions further comprise instructions for:

in the deactivating, configuring a system timer to send a first timer interrupt after the dynamic variable amount of time has elapsed, the dynamic variable amount of time being a maximum amount of time that a first thread can yield to a second thread before the first thread needs to be executed(col. 3 lines 15-34); and

responsive to receiving the first timer interrupt:

(a) configuring the system timer to send a second timer interrupt at the periodic rate (col. 3 lines 15-34); and

(b) activating the deactivated at least one subset of components to determine if there are any threads to execute (col. 3 lines 15-34).

28. As per claim 20, Toll teaches the invention as claimed, including a computer-readable storage medium as recited in claim 15, wherein the computer-executable instructions further comprise instructions for:

receiving an external interrupt before the dynamic variable amount of time has elapsed since the deactivating, the external interrupt not being a system timer interrupt (col. 3 lines 15-34); and

responsive to receiving the external interrupt, processing the external interrupt such that the at least one subset of components remain deactivated for the dynamic variable amount of time (col. 3 lines 15-34).

29. As per claim 21, Toll teaches the invention as claimed, including a computer comprising one or more computer-readable media as recited in claim 15 (Claim 21).

30. As per claim 22, Toll teaches the invention as claimed, including a device comprising:

a processor configured to fetch and execute a plurality of computer-executable instructions (col. 1 lines 11-24; col. 1 lines 32-46);

a plurality of hardware elements coupled to the processor (col. 1 lines 11-24; col. 1 lines 32-46); and

a memory coupled to the processor for storing the computer-executable instructions comprising a scheduler program module, a hardware abstraction layer (HAL) program module, one or more operating system program modules, and a set of application program modules (col. 1 lines 11-24; col. 1 lines 32-46);

wherein the scheduler comprises computer-executable instructions for:

scheduling threads for execution at a periodic time interval (col. 2 lines 22-28; col. 3 lines 38-45); and

determining that there are no threads to execute (col. 2 lines 32-34; col. 3 lines 8-12);

wherein the HAL, responsive to the determining, comprises computer-executable instructions for deactivating, for a dynamic variable amount of time (col. 2 lines 32-34; col. 3 lines 8-12), at least one subset of components selected from a group of components comprising the scheduler, the hardware elements, the one or more operating system program modules, and the application program modules (col. 2 lines 32-34), the dynamic variable amount of time being independent of the periodic time interval and being based on a sleep state of a set of threads (col. 3 lines 23-30).

31. The absence of a teaching of a "sleep queue" within Toll is discussed above in reference to paragraph 9.

32. As per claim 23, Toll teaches the invention as claimed, including a device as recited in claim 22, wherein the dynamic variable amount of time is based on a maximum amount of time that a thread can yield before needing to be scheduled (col. 3 lines 15-18; col. 3 lines 30-34).

33. As per claim 25, Toll teaches the invention as claimed, including a device as recited in claim 22, wherein the device comprises a battery powered device (col. 1 lines 11-24).

34. As per claim 26, "Official Notice" is taken that the use of the Microsoft WINDOWS CE, Linux, WindRiver, QNX, or Palm operating systems would have been an obvious modification to Toll for reasons discussed above in reference to paragraph 12.

35. As per claim 27, Toll teaches the invention as claimed, including a device as recited in claim 22, wherein the HAL further comprises computer-executable instructions for re-activating the at least one subset of components after the dynamic variable amount of time has elapsed since the at least one subset of components were deactivated (col. 3 lines 15-34).

36. As per claim 28, Toll teaches the invention as claimed, including a device as recited in claim 27, wherein the scheduler is re-activated in a manner that allows the scheduler to schedule threads based on the periodic time interval (col. 3 lines 15-34).

37. As per claim 29, Toll teaches the invention as claimed, including a device as recited in claim 22, wherein after the scheduler is deactivated, the HAL further comprises computer-executable instructions for receiving a notification in response to an external event, the external event not being a system timer event, responsive to receipt of the notification, the HAL processing the notification in a manner that the scheduler remains deactivated for the dynamic variable amount of time (col. 3 lines 15-34).

38. **Claims 5, 11, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toll in view of Harris et al. (USPN 6,438,704) (hereinafter Harris).**

39. As per claim 5, Harris teaches the invention as claimed, including the following limitations not shown by Toll:

a method as recited in claim 1, wherein the predetermined periodic rate is a millisecond (col. 6 lines 30-40; col. 10 line 65 - col. 11 line 13).

40. It would have been obvious to one of ordinary skill in the art to combine Toll and Harris since operations that may be CPU bound and require little time waiting for external events, such as synchronization or waiting for shared data, can be executed in quick time slices, such as one millisecond (Harris, col. 11 lines 6-13). The use of shorter timeslices for threads that are not waiting on events allows for the thread to complete its work faster, and thus completing its work and allowing the computer to go into a low power mode to conserve battery life (Toll, col. 1 lines 11-24).

41. As per claim 11, Harris teaches the invention as claimed, including a method as recited in claim 8, wherein the predetermined periodic rate is a millisecond (col. 6 lines 30-40; col. 10 line 65 - col. 11 line 13).

42. As per claim 24, Harris teaches the invention as claimed, including a device as recited in claim 22, wherein the periodic time interval is a millisecond (col. 6 lines 30-40; col. 10 line 65 - col. 11 line 13).

***Conclusion***

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fung (USPN 6,079,025; 6,584,571) teach a method of conserving battery power by reducing clock speed when threads are sleeping.

Watts, Jr. (USPN 6,158,012) and Watts, Jr. et al. (USPN 6,173,409) teach a real-time computing method of power conserving that utilizes a monitor to sample CPU activity in making a determination of whether or not to enter a low power mode.

Esfahani (USPN 6,438,668) teaches a method of reducing power consumption in a computer.

Ewertz (USPN 6,499,102) teaches preserving battery power when a computer has entered a sleep state.

Zolnowsky (USPN 6,779,182) teaches the use of sleep queues for preparing threads that are blocked or awaiting synchronization on an object.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
August 23, 2004

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